CLAIMS:

1. A switched capacitor circuit formed on a substrate of a semiconductor integrated circuit, comprising:

an MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in a plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of the top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; and a capacitor.

2. The circuit according to claim 1, wherein

a channel is formed on a first crystal surface of a top surface and a second crystal surface of a side surface of the projecting portion, and the channel width of the MIS field-effect transistor is a total of a channel width of the top surface and a channel width of the side surface.

3. The circuit according to claim 1 or 2, wherein the projecting portion has a top surface comprising a silicon surface (100), the side surface comprising a silicon surface (110), and the source and drain are formed on the projecting portion enclosing the gate and in left and right areas of the projecting portion of the silicon substrate.

4. The circuit according to claim 1 or 2, wherein the switched capacitor circuit comprises a switch formed by connecting in parallel a p-channel MIS field-effect transistor and n-channel MIS field-effect transistor, and a gate width of a top surface and the side surface of the projecting portion of the p-channel MIS field-effect transistor is set such that current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

5. The circuit according to claim 1 or 2, wherein the switched capacitor circuit comprises: first p-channel and n-channel MIS field-effect transistors which receive a signal at an input terminal, and are

connected in parallel to each other; second p-channel and n-channel MIS transistors which are connected to each other, whose input terminals are connected to output terminals of the first p-channel and n-channel MIS field-effect transistor, and whose output terminals are grounded; a capacitor one terminal of which is connected to an output terminal of the first p-channel and n-channel MIS field-effect transistors; third p-channel and n-channel MIS field-effect transistors which are connected in parallel to each other, whose input terminal is connected to another terminal of the capacitor, and whose output terminal is grounded; and fourth p-channel and n-channel MIS field-effect transistors which are connected in parallel to each other and whose input terminal is connected to another terminal of the capacitor.

6. A semiconductor integrated circuit, comprising:

a circuit comprising a p-channel MIS field-effect transistor and an n-channel MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in plasma atmosphere of an inert gas, then a gate

insulating film is formed on at least a part of the top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; and a switched capacitor circuit comprising the p-channel MIS field-effect transistor or the n-channel MIS field-effect transistor and a capacitor.

7. The circuit according to claim 6, wherein gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

8. The circuit according to claim 6 or 7, wherein the switched capacitor circuit comprises a switch formed by connecting in parallel the p-channel MIS field-effect transistor with the n-channel MIS field-effect transistor.